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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,141	06/27/2003	Jonathan M. Haswell	FIS920030157	1140

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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,141	HASWELL ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/27/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on June 27, 2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Oath/Declaration

The Oath filed June 27, 2003 complies with all the requirements set forth in MPEP 602 and therefore is accepted.

Drawings

The drawings filed January 16, 2004 are accepted.

Specification

The specification filed June 27, 2003 has a blank page 11 and page 10 has information in the center of the page. Applicants are requested to delete the blank page 11 and move the information of page 10 to the top of the page. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claim 16 is objected to because of the following informalities:

- The term "tangibly" need not to be in the claim language as it is not a positive limitation. The Examiner would like to point out that the claim would remain statutory under 35 USC 101 without this term, due to "...program storage device...".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites, "...the raw data signal including an error detection code..." which is confusing because by definition raw data has to be data which is not processed. Seemingly, Applicants are using the term raw data repugnant to the definition customarily used for raw data. As a result, Examiner cannot give patentable weight to the term raw data.

Claims 11 and 16 have similar problems as pointed out in claim 1 and the same shall be done for them as well.

Claim 2 recites the limitation "the original raw data" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 16 recites the limitation "the machine" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto (USPN 4617660) further in view of Albonesi (USPN 4920539).

As per claim 1, Sakamoto substantially teaches a faulty-memory processing method and apparatus in a data processing system which executes a time-sharing data process with breaks. Hard error which may exist in a cell in a normal memory is detected by using an error correction circuit. After correcting an error in information read out from a detected hard-error cell in the normal memory, information including the above corrected information with respect to the detected hard-error cell is transcribed into a relief memory. The above correction and transcription is executed during the breaks in the time-sharing data process. Sakamoto teaches (Figure 1) a data processing system fundamentally has a CPU, a memory unit (MU), and data channel units (DCH), connected to each other by a common bus. Input/output (I/O) devices are coupled to the data channel units. The CPU performs data processing in cooperation with the MU. The DCH's control the I/O devices with respect to the MU. The MU includes an error

detecting circuit for detecting errors in read and write data with respect to the MU and an error correcting circuit for automatically correcting the detected error. Sakamoto teaches (col. 11, lines 21-46) a faulty memory processing method in a data processing system including memory means having a normal memory with a plurality of cells for storing information, a relief memory, and error correction means for detecting and correcting an error in information read out from at least one cell in said normal memory, said data processing system executing a time-sharing data process with time period breaks, said faulty-memory processing method comprising the steps of: detecting a hard error which may exist in at least one cell in said normal memory, said detection being carried out using said error correction means; correcting, using said error correction means, an error in information read out from a detected hard error cell of the normal memory; transcribing information including the corrected information with respect to the detected hard-error cell of the normal memory into the relief memory, said correcting and transcribing steps being executed during the time period breaks in said time-sharing data process; and processing in a normal mode where data read out from the memory means are immediately utilized without waiting for the detection and correction performed by the error.

Sakamoto does not explicitly teach to check the data signal for corruption at the time it is received by the computer processor as stated in the present application.

However, Albonesi teaches, in an analogous art, (col. 8, lines 11-29) a computer system having a processing unit, memory, memory control unit, system communication bus, and bus control unit, a method of correcting memory errors, comprising the steps of, detecting a data error while data is being transferred from the memory to the system bus and generating corresponding corrected data if a data error is detected, storing at the memory control unit at

least the address field and source identification code associated with the just detected data error, generating a bus request signal coupled to the bus control unit, said bus control unit, in turn, generating a bus grant signal, said memory control unit in response to said bus grant signal issuing a read message on the system bus having an address field and destination identification code corresponding to said stored address field and source identification code, and in response to said read message, the device indicated by said identification code, writing back to memory the correct data corresponding to said address field. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the checking of the data signal for corruption at the time it is received by the computer processor within the method and apparatus of Sakamoto. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by checking the data signal for corruption at the time it is received by the computer processor would have relieved the memory of such detection and correction process and hence enhanced the system.

As per claims 2, 12 and 17, Sakamoto substantially teaches (col. 4, lines 53-62), in view of above rejections, to determine if the corrupted data may be corrected.

As per claims 3, 5, 14 and 18, Sakamoto substantially teaches (Figure 4 and col. 5, lines 22-41), in view of above rejections, the computer processor or CPU to determine if the received signal is corrected.

As per claims 4 and 19, Sakamoto substantially teaches (Figure 5), in view of above rejections, the corrected data to be rewritten to the memory.

As per claims 6-7 and 13, Sakamoto substantially teaches (Figure 7 and associated text), in view of above rejections, for each memory element of a dynamic RAM, the refresh operation

is periodically executed in response to the refresh timing signal S.sub.f. FIG. 7 indicates a memory cell array of a dynamic RAM of 256 K bit. In this RAM, all cells (1024 bits) in a column are simultaneously refreshed at an interval of 15 msec. All cells in the RAM (256 columns) will be refreshed in about 4 msec. As is known, in FIG. 7, if a refresh address (column address) of "2" and a row address of "3" are applied to the RAM, the contents in a cell 18 are read out.

As per claims 8-10 and 15, Albonesi substantially teaches, in view of above rejections, (col. 8, lines 11-29) a computer system having a processing unit, memory, memory control unit, system communication bus, and bus control unit, a method of correcting memory errors, comprising the steps of, detecting a data error while data is being transferred from the memory to the system bus and generating corresponding corrected data if a data error is detected, storing at the memory control unit at least the address field and source identification code associated with the just detected data error, generating a bus request signal coupled to the bus control unit, said bus control unit, in turn, generating a bus grant signal, said memory control unit in response to said bus grant signal issuing a read message on the system bus having an address field and destination identification code corresponding to said stored address field and source identification code, and in response to said read message, the device indicated by said identification code, writing back to memory the correct data corresponding to said address field.

As per claim 11, Sakamoto substantially teaches a faulty-memory processing method and apparatus in a data processing system which executes a time-sharing data process with breaks. Hard error which may exist in a cell in a normal memory is detected by using an error correction circuit. After correcting an error in information read out from a detected hard-error cell in the

normal memory, information including the above corrected information with respect to the detected hard-error cell is transcribed into a relief memory. The above correction and transcription is executed during the breaks in the time-sharing data process. Sakamoto teaches (Figure 1) a data processing system fundamentally has a CPU, a memory unit (MU), and data channel units (DCH), connected to each other by a common bus. Input/output (I/O) devices are coupled to the data channel units. The CPU performs data processing in cooperation with the MU. The DCH's control the I/O devices with respect to the MU. The MU includes an error detecting circuit for detecting errors in read and write data with respect to the MU and an error correcting circuit for automatically correcting the detected error. Sakamoto teaches (col. 11, lines 21-46) a faulty memory processing method in a data processing system including memory means having a normal memory with a plurality of cells for storing information, a relief memory, and error correction means for detecting and correcting an error in information read out from at least one cell in said normal memory, said data processing system executing a time-sharing data process with time period breaks, said faulty-memory processing method comprising the steps of: detecting a hard error which may exist in at least one cell in said normal memory, said detection being carried out using said error correction means; correcting, using said error correction means, an error in information read out from a detected hard error cell of the normal memory; transcribing information including the corrected information with respect to the detected hard-error cell of the normal memory into the relief memory, said correcting and transcribing steps being executed during the time period breaks in said time-sharing data process; and processing in a normal mode where data read out from the memory means are immediately utilized without waiting for the detection and correction performed by the error.

Sakamoto does not explicitly teach to check the data signal for corruption at the time it is received by the computer processor as stated in the present application.

However, Albonesi teaches, in an analogous art, (col. 8, lines 11-29) a computer system having a processing unit, memory, memory control unit, system communication bus, and bus control unit, a method of correcting memory errors, comprising the steps of, detecting a data error while data is being transferred from the memory to the system bus and generating corresponding corrected data if a data error is detected, storing at the memory control unit at least the address field and source identification code associated with the just detected data error, generating a bus request signal coupled to the bus control unit, said bus control unit, in turn, generating a bus grant signal, said memory control unit in response to said bus grant signal issuing a read message on the system bus having an address field and destination identification code corresponding to said stored address field and source identification code, and in response to said read message, the device indicated by said identification code, writing back to memory the correct data corresponding to said address field. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the checking of the data signal for corruption at the time it is received by the computer processor within the method and apparatus of Sakamoto. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by checking the data signal for corruption at the time it is received by the computer processor would have relieved the memory of such detection and correction process and hence enhanced the system.

As per claim 16, Sakamoto substantially teaches a faulty-memory processing method and apparatus in a data processing system which executes a time-sharing data process with breaks.

Hard error which may exist in a cell in a normal memory is detected by using an error correction circuit. After correcting an error in information read out from a detected hard-error cell in the normal memory, information including the above corrected information with respect to the detected hard-error cell is transcribed into a relief memory. The above correction and transcription is executed during the breaks in the time-sharing data process. Sakamoto teaches (Figure 1) a data processing system fundamentally has a CPU, a memory unit (MU), and data channel units (DCH), connected to each other by a common bus. Input/output (I/O) devices are coupled to the data channel units. The CPU performs data processing in cooperation with the MU. The DCH's control the I/O devices with respect to the MU. The MU includes an error detecting circuit for detecting errors in read and write data with respect to the MU and an error correcting circuit for automatically correcting the detected error. Sakamoto teaches (col. 11, lines 21-46) a faulty memory processing method in a data processing system including memory means having a normal memory with a plurality of cells for storing information, a relief memory, and error correction means for detecting and correcting an error in information read out from at least one cell in said normal memory, said data processing system executing a time-sharing data process with time period breaks, said faulty-memory processing method comprising the steps of: detecting a hard error which may exist in at least one cell in said normal memory, said detection being carried out using said error correction means; correcting, using said error correction means, an error in information read out from a detected hard error cell of the normal memory; transcribing information including the corrected information with respect to the detected hard-error cell of the normal memory into the relief memory, said correcting and transcribing steps being executed during the time period breaks in said time-sharing data process; and processing

in a normal mode where data read out from the memory means are immediately utilized without waiting for the detection and correction performed by the error.

Sakamoto does not explicitly teach to check the data signal for corruption at the time it is received by the computer processor as stated in the present application.

However, Albonesi teaches, in an analogous art, (col. 8, lines 11-29) a computer system having a processing unit, memory, memory control unit, system communication bus, and bus control unit, a method of correcting memory errors, comprising the steps of, detecting a data error while data is being transferred from the memory to the system bus and generating corresponding corrected data if a data error is detected, storing at the memory control unit at least the address field and source identification code associated with the just detected data error, generating a bus request signal coupled to the bus control unit, said bus control unit, in turn, generating a bus grant signal, said memory control unit in response to said bus grant signal issuing a read message on the system bus having an address field and destination identification code corresponding to said stored address field and source identification code, and in response to said read message, the device indicated by said identification code, writing back to memory the correct data corresponding to said address field. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the checking of the data signal for corruption at the time it is received by the computer processor within the method and apparatus of Sakamoto. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by checking the data signal for corruption at the time it is received by the computer processor would have relieved the memory of such detection and correction process and hence enhanced the system.

As per claim 20, Sakamoto substantially teaches, in view of above rejections, (col. 1, lines 14-32) a memory unit in a data processing system is provided with a function for detecting an error in data read from the memory unit and for correcting the detected error by an error correcting code (ECC).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2133
September 14, 2005

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
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